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Supreme Court, U.S.
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No. _____

In the

SUPREME COURT OF THE UNITED STATES

ALL COMPUTERS, INC.,

Petitioner,

v.

INTEL CORPORATION,

Respondent.

On Petition for a Writ of Certiorari to the United States Court Of Appeals for the Federal Circuit No. 07-1016

PETITION FOR WRIT OF CERTIORARI

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QUESTIONS PRESENTED FOR REVIEW

In a patent infringement action, on a motion for summary judgment can a court interpret claims including technical terms without relying on expert testimony or without an evidentiary hearing including expert testimony?

RULE 14.1(b) STATEMENT AND CORPORATE DISCLOSURE STATEMENT UNDER RULE 29.6

Counsel for the Petitioner, All Computers, Inc.,

1. A list of all parties to the proceeding certifies the following: in the court whose judgment is the subject of this petition is included in the caption of the case.

2. The full name of every party or amicus represented by me is All Computers, Inc., which is the real party in interest.

3. No parent corporation or publicly held company owns 10 percent or more of the stock of All Computers, Inc.

December 12, 2007

_____

Michael P. Fortkort
Attorney for Appellant, All Computers, Inc.

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PETITION FOR A WRIT OF CERTIORARI

Petitioner, All Computers, Inc. ("ACI") respectfully petitions for a writ of certiorari to review the judgment of the U.S. Court of Appeals for the Federal Circuit affirming the lower court's grant of summary judgment of non-infringement without opinion.

OPINIONS BELOW

The Judgment of the Court of Appeals for the Federal Circuit denying Petitioner's Petition for Rehearing is reproduced at Appendix A1-A2.

The Judgment of the Court of Appeals for the Federal Circuit affirming the District Court's summary judgment is reproduced at App. B1.

The Final Judgment, Judgment and Memorandum Opinion and Order of the U.S. District Court for the Eastern District of Virginia is reproduced at App. C1-C40.

JURISDICTION

On May 18, 2007 the judgment sought to be reviewed was entered by the Court of Appeals for the Federal Circuit affirming the District Court's judgment. The decision on Petitioner's petition for rehearing that was timely filed and/or entertained by the Court of Appeals for the Federal Circuit was

entered on July 12, 2007. This Court's jurisdiction is invoked under 28 U.S.C. § 1254(1). This petition is timely under 28 U.S.C. § 2101(c) and Supreme Court Rule 13.3 because it is being filed within 90 days of the date of denial of rehearing on petitioner's motion for rehearing entertained by the Court of Appeals of the Federal Circuit.

The District Court had jurisdiction to hear Petitioner's claim for patent infringement under 28 U.S.C. § 1338(a). The Court of Appeals for the Federal Circuit had jurisdiction to hear Petitioner's appeal under 28 U.S.C. § 1295(a)(1).

STATUTORY PROVISIONS INVOLVED

The relevant statutory provisions involved are Fed.R.Civ.P. 56(c).

STATEMENT OF THE CASE

This case raises questions of broad and general importance: What is the proper reliance on expert testimony when interpreting claims of a validly issued patent; and is an evidentiary hearing required when construing complex claims? The answer to these questions affects every U.S. federal court assertion of infringement. It is a matter of concern to every company and member of the public affected by the grant of a U.S. patent.

Petitioner is the owner by assignment of U.S. Patent No. 5,506,981 ("the '981 patent") entitled "Apparatus and Method for Enhancing the

Performance of Personal Computers." Petitioner alleges that certain of Respondent Intel products, including it Celeron® Products infringe Claims 1, 3 and 5 of the '981 patent.

The District Court entered summary judgment of non-infringement based on certain erroneous rulings of claims construction.

Petitioner appealed the District Court's summary judgment of non-infringement and its rulings of claim construction. The Court of Appeals affirmed the District Court's judgment without opinion. Petitioner sought reconsideration of the affirmance, but again was denied without opinion.

REASONS FOR GRANTING THE PETITION

The Court of Appeals has sanctioned a departure that is so far from the accepted and usual course of judicial proceedings by a lower court as to call for this Court's supervisory power.

The District Court granted summary judgment based on three claim construction rulings that required detailed knowledge of the technology at issue without the benefit of an evidentiary hearing or the testimony of an expert in support of these rulings. In fact, the only expert involved, Petitioner's expert, submitted an affidavit inapposite to the court's claim construction rulings. No expert opinion or testimony was submitted in support of the motion for summary judgment by Respondent Intel. The lower court rejected the expert's opinions as unreliable without viewing the

demeanor of the expert, as only snippets from the expert's deposition were supplied to the court. In short, the lower court substituted its judgment for that of the expert. This departs dramatically from accepted practice on issues involving experts. Without exercising its supervisory powers, lower courts will continue to issue claim construction rulings of complex technology without the benefit of expert opinion as this has now been sanctioned by the Court of Appeals. In fact, some District Courts (but not others) employ a so-called Markman hearing to ascertain the meaning of claims, which Markman hearing is an evidentiary hearing. No such hearing was employed in this case and none is required by the Court of Appeals. In the instant case, only briefs were supplied to the District Court.

Secondly, the District Court granted summary judgment while presumably invoking the standard of reviewing the alleged facts in the light most favorable to the non-moving party yet completely disregarded Petitioner's expert testimony in support of facts supporting claim construction in complete disregard for the appropriate standard of review.

The District Court overlooked the requirement that summary judgment of non-infringement can only be granted if, after viewing the alleged facts in the light most favorable to the non-movant, there is no genuine issue whether the accused device is encompassed by the claims. *See*

Fed.R.Civ.P. 56(c); *Anderson v. Liberty Lobby, Inc.*, 477 U.S. 242, 255, 106 S.Ct. 2505, 91 L.Ed.2d 202 (1986). Concomitant with this requirement is that all reasonable factual inferences must be construed in the non-movant's favor. *See National Recovery Techs., Inc. v. Magnetic Separation Sys., Inc.*, 166 F.3d 1190, 1194, 49 USPQ2d 1671, 1674 (Fed.Cir.1999). When applying these core legal principles to the facts herein, summary judgment should be denied.

When discussing the proper analysis on a motion for summary judgment, the Federal Circuit recently stated in *Pitney Bowes, Inc. v. Hewlett Packard Co.:*

> Summary judgment of non-infringement requires a two-step analytical approach. First, the claims of the patent must be construed to determine their scope. *See Carroll Touch, Inc. v. Electro Mechanical Sys.*, Inc., 15 F.3d 1573, 1576, 27 USPQ2d 1836, 1839 (Fed.Cir.1993). Second, a determination must be made as to whether the properly construed claims read on the accused device. *See id.* The first step of this analysis-claim construction is a question of law. See *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979, 34 USPQ2d 1321, 1329 (Fed.Cir.1995) (*in banc*), aff'd, 517 U.S. 370, 116 S.Ct. 1384, 134 L.Ed.2d 577 (1996). Accordingly, it

falls upon the district court to discern the meaning of the claim language. *See id.* Because it is a legal question, our review of the district court's claim construction is de novo. *See Cybor Corp. v. FAS Techs., Inc.*, 138 F.3d 1448, 1456, 46 USPQ2d 1169, 1174 (Fed.Cir.1998) (in banc).

Thus, summary judgment of non-infringement can only be granted if, after viewing the alleged facts in the light most favorable to the non-movant, there is no genuine issue whether the accused device is encompassed by the claims. *See* Fed.R.Civ.P. 56(c); *Anderson v. Liberty Lobby, Inc.*, 477 U.S. 242, 255, 106 S.Ct. 2505, 91 L.Ed.2d 202 (1986). Consequently, when summary judgment of non-infringement has been granted based upon undisputed material facts, our review of the district court's application of this second analytical step is de novo, construing, once more, all reasonable factual inferences in the non-movant's favor. *See National Recovery Techs., Inc. v. Magnetic Separation Sys., Inc.*, 166 F.3d 1190, 1194, 49 USPQ2d 1671, 1674 (Fed.Cir.1999). 182 F.3d 1298, 1304 (Fed. Cir. 1999).

182 F.3d 1298, 1304 (Fed. Cir. 1999).

The District Court's summary judgment decision fails to apply this standard to the facts of this case. In particular, the District Court appears to have decided facts in favor of the moving party, Intel, rather than viewing the facts in the light MOST FAVORABLE to the non-moving party. As the Court of Appeals has affirmed the District Court's opinion *per curiam*, ACI can only presume the Court of Appeals has completely adopted the District Court's opinion.

For this reason, Petitioner petitions for a writ of certiorari by this Court. No issues of fact were viewed in the light most favorable to ACI and no factual inferences were construed in favor of ACI.

A. Direct Infringement Occurred and is Continuing

To support a claim for contributory or inducing infringement, the District Court examined the evidence of direct infringement. Under this analysis, the District Court failed to view the facts from ACI's expert in the light most favorable to ACI.

ACI's expert discussed a certain document (Intel "PC Buying Tips", A0052), which he claimed showed direct infringement supporting claims for inducing or contributory infringement.

But in its decision, the District Court did not even cite the facts most favorable to ACI when reading the Intel "PC Buying Tips" document (A0052). The District Court's opinion only included

lines 3-5 of the last paragraph of page 1 of this document, which the District Court used to support its decision that there was no direct infringement.

The District Court failed to include the next four lines of this paragraph, which are contrary to its decision. Lines 6-9 of the last paragraph on page 1 state:

> Purchasing a motherboard based on an Intel chip set (such as an Intel-built motherboard), gives you the added benefit of knowing that its core components have gone through rigorous validation with a large range of industry devices and software, so you know it will have rock-solid dependability.

These lines prove that Intel manufactures motherboards, then rigorously tests and validates the finished product, and sells them to users in large quantities, as indicated in column 5 of their "Calculation of Accused Chips Revenue" (A0996), and thereby establishes direct infringement.

The Celeron processor is mounted on an Intel motherboard along with the clock chip. This combination is therefore sold by Intel and used by Intel's customers, hence there exists direct infringement. The District Court completely disregarded this evidence to conclude no direct infringement occurred when dismissing the claims for contributory and inducing infringement. In

short, the facts on this issue were not properly viewed and all reasonable inferences not taken in ACI's favor.

Next we shall address the three reasons the lower court cites for non-infringement (A0022). ACI draws supporting data from Defendant Counsel's false and incorrect statements made at the Oral Hearing as well as a few other noteworthy items in the record to add further clarity to this omission of application of the most favorable light and reasonable inference construction standards.

B. Accelerator Board Need Not Include Board1.

1. *Claim Construction of Accelerator Board*

When analyzing literal infringement, the District Court needed to construe the claim term "accelerator board" to determine whether "accelerator board" included a "board." Here the District Court noted the parties disputed this, with Intel arguing the term must specifically include a printed circuit board (PCB) as the "board" and ACI arguing the broader definition of "board," which can include any of a number of substrates in addition to the PCB's resin and plastic.

While the court's construction of a claim term is a matter of law, *Markman*, 52 F.3d at 979, 34 USPQ2d at 1329, the District Court's construction relies upon facts, which the court failed to view in the light most favorable to ACI.

For example, the District Court noted that

ACI's expert "admitted then attempted to retract his opinion that the accelerator board contained a board." (A0047). Yet, the District Court could have viewed this fact as the uncontested opinion of ACI's expert – Intel did not provide any evidence from an expert. By analyzing the facts in this manner, the District Court appeared to be weighing the evidence as a factfinder rather than analyzing summary judgment issues. In fact, a careful reading of the lower court's opinion makes one think a full evidentiary hearing was held on these issues, with the court weighing the credibility of the witnesses. Such was not the case, and hence summary judgment is not proper under these circumstances.

Also, upon reading Intel's citations from Dr. Smith's transcript in their Summary Judgment Memorandum (A0577 – A0580), it turns out Dr. Smith was not retracting at all. The only person playing word games is Intel's counsel. The final question (A0580) tells all:

Q. Now, in the case of an accelerator board that is made out of a PCB with components on it.....then you have an upgrade processor. Correct?

A. It could be designed that way, yes.

Q. But the Celeron chip is not designed that way. Correct?

A. That's my understanding. Correct.

Here Intel counsel finally uses the word "chip" with "Celeron," however it is an attempt to get in through the back door, but he does not catch

Dr. Smith. Clearly the Celeron microprocessor chip does not have a board (PCB) – but the "Celeron" or "Celeron" product, or Celeron module or Celeron board does. The lower court accused Dr. Smith of word-smithing, but the only real examples we see is that of Intel's counsel.

2. *But Accused Device Includes a Board*

Furthermore, the District Court stated that the "parties do not dispute that the accused Intel Celeron microprocessor is not mounted on an accelerator board, as there is no second printed circuit board." (A0048). In fact, the parties do dispute this fact, which alone should prevent granting of summary judgment of non-infringement.

Nevertheless, ACI can show that when viewing the facts in the light most favorable to ACI along with construing all reasonable inferences in ACI's favor, the accused Celeron does include a board.

Consider Intel Counsel's statement made during the Oral Hearing, which ACI submits is clearly false.

"No" [Intel counsel's response to a question from the Panel "so is the Celeron something that has all the components ... so it really is a board?"] (Audio 16:10 – 16:20).

Essentially, Intel counsel stated that the Celeron does not include a board. But all present at the Oral Hearing saw a Celeron board. Also, two other samples of Celeron/Pentium devices were sent to the Court with ACI's brief along with two

pictures included in Mr. Kutt's declaration (A1103) showing various versions of Celerons and Pentiums each with a microprocessor chip mounted on the boards.

The District Court simply rejected this evidence rather than viewing it in the light most favorable to ACI. Again, if the District Court properly viewed the accused products as is the custom if not the requirement, it would have denied the motion on this ground.

Moreover, even the Court of Appeals noted the presence of a dispute on this fact because the Appeals Panel asked Intel's counsel this very question during oral argument, which counsel could only respond to with a "No" (i.e., Celerons do not include a board) without further explanation. This false statement may have misled the Court of Appeals for the reasons cited above. As such, when the facts are properly viewed in the light most favorable to ACI, this Court should remand this case to the lower court for an evidentiary hearing on whether Celerons do include a board.

This false statement dealt with the heart of the Defendant's public strategy over the past 12 years to hide the presence of a board in all Celerons, thereby letting confusion reign.

ACI believes with strong conviction that the correct answers on these matters at the Oral Hearing would have had led the Court of Appeals to a reversal decision. ACI provides further support for its conviction below.

Some of this exposed data came to light in

the Fees Hearing, at which ACI prevailed, and so surprised the Magistrate Judge that he commented at the end of the Hearing that earlier knowledge of this information would have had a decided impact at the Summary Judgment Hearing.

The District Court had been led to believe that the Celeron was a chip and that there was no board; however, for the first time the District Court actually got to see Celeron boards, including the accused product – and these boards all had a Celeron or Pentium microprocessor chip mounted thereon.

Celeron and Pentium microprocessor chips are in fact identical. Mr. Keng Wong, the senior engineer in clock circuits for Intel, confirmed in his deposition that Intel marketing assigned the two names to the same microprocessor chip.

Plaintiff Attorney Q. "Why does Intel - - how does Intel determine whether they are going to call them a Pentium 4 or a Celeron?"

Wong A. "That's a marketing question."

In other words they are identical microprocessor chips. (A1035: Wong p 51).

The significance of the last two statements is that proving that the Celeron and ICS chip infringe necessarily implies first that all the sister Pentiums also infringe. As a result, we urge this Court to revisit the sanction as we believe that it was improperly imposed, contrary to the required process as outlined in the ACI brief page 53.

With these new findings and the Defendant's loss of credibility, the case can finally be reviewed

without a cloud of confusion. All Celerons and Pentiums have a board, all Celeron microprocessor chips have the traditional CPU plus the new infringing upgrade circuitry; all Celerons have the remaining clock circuitry in the clock chip. ACI's expert reiterated this with backup throughout (and all reference locations in bold, as are the following, are under oath and penalty of perjury). (A0955: F) and (A0957: L, M).

"Accelerator board is not an accelerator board, not a single edge connector board at all, in fact what it was, was the ACS clock chip, I'm sorry, the ICS9250-10 clock chip..." (Audio 16:50-17:25)

Essentially, Intel counsel claimed that ACI said "the accelerator board is an ICS clock chip!" Of course both items are false. ACI never said this and the accelerator board is obviously not a clock chip (A0955: D) and (A0956: I).

C. Accused Device Includes First Clock Signal

Under this prong of the District Court's analysis, the District Court identified the factual dispute, i.e., Intel argues that its accused system has no first clock signal, whereas ACI responded with multiple arguments to the contrary. (A0957: K, O) and (A0958: R). As this is a factual issue in dispute, summary judgment was not proper.

Furthermore, the District Court again failed to view the facts in the light most favorable to ACI. Moreover, the court resolves this disputed issue of fact during its opinion, in which it seems to be

acting as a fact-finder rather than deciding a summary judgment motion. Simply put, summary judgment is not the proper time for determination of these disputed facts.

Again, the Court should consider comments made by Defense Counsel during the Oral Hearing, in which he stated:

> The clock signal, that ACI points to as being the first clock signal, never escapes the clock chip, it is buried in the circuitry of the clock chip and it cannot be used in the processor ...it can never be used outside because it never gets out of the clock chip. (Audio 20:55 – 21:25).

Essentially, Intel counsel is saying that the signal named first clock never leaves the clock chip – and that part is at least correct to the extent that the name is not used outside of the clock chip and the frequency changes. Otherwise the signal's control survives as the diverse signals that are derived from it operates the diverse devices in the computer, including the first and second microprocessors.

This is one of the most basic rules of PC design. A single 'system' clock derived from a single crystal oscillator controls and operates the microprocessor chip, as well as the rest of the slower devices in the computer. Intel's introduction of the brief, Intel reinforces the above facts - prior art used "free running" clocks which proved to be

too slow because the process of synchronizing independent clocks "was time consuming" (Intel Brief: 4 lines 1-7) and "for the new microprocessor to communicate with the rest of the system the accelerator clock had to be synchronized with the system board clock." (Intel Brief: 4 lines 3-5). Intel's brief then explained that the solution was to derive the faster clocks from the original clock (Intel Brief: 4 line 12). The brief then defines "known phase relationship" as "the phase difference between the two signals is zero, or at least known so that the appropriate correction can be made."

The District Court interpreted the phase difference between the two signals is zero; however, only the latter portion of the definition (i.e., at least known so that the appropriate correction can be made) applies because zero only applies when the two signals have the same frequency, which is clearly not the case.

Intel also presents a good example, where the new signal's frequency is three times the old (Intel Brief: 7, 4-6). In this description there was no need for the first clock signal to leave the clock chip because the signals derived from it, as just described, is in fact the optimum way to synchronize with the higher, second clock frequency – that is, with a known phase relationship.

Therefore, when the facts are viewed in the most favorable light to ACI, there exists a first clock signal within the meaning of the claims at issue.

D. Known Phase Relationship Exists in Accused Device

In this aspect of the District Court's opinion on non-infringement, the District Court determined that Intel's accused products do not have a known phase relationship with their system as required by the claims at issue. This remains a disputed fact, the adjudication of which is not proper at the summary judgment stage.

In fact, the opposite is true as explained in the previous section, in Dr. Smith's sworn declaration (A0957: U) and (A059: V), and as further confirmed in the Oral Hearing at the Court of Appeals during which Intel's Counsel stated:

"[ACI] now understand[s] that the Intel system doesn't have these known phase relationships" (Audio 20:35 – 20:55).

Intel counsel alleges that ACI said that "ACI understands that the Intel system", not merely the Celeron processors, "do not have known phase relationships." Had ACI said this, it would have been false! But ACI did not state this.

The ICS clock chip document shows this falsity as it clearly shows that there are at least another 8 PCI clock signals that have a known phase relationship with the three copies of the CPU clock signal, which is the sub-harmonic clock signal (also referred to as CPU66/100[2:0] MHz). The Block Diagram (A0908) shows that exiting the chip on the right side are the eight PCICLK[7:0] clock signals (7th line) and the 3 CPU66/100 clock signals (3rd line). The Features Table on the same page

confirms that clock chip "generates" respectively the eight and three copies of the two clock signals (lines 6 and 3). The Pin Description table (A0909) completes the proof as it indicates opposite the Pin Name 'PCICLK[7:0] (8th Pin Name line) that the Description of these signals is "3.3 V PCI clock outputs, with synchronous CPUCLKS." They are synchronous and therefore the synchronization takes place with a known phase relationship.

As ACI definitely did not make the alleged statement, Intel's statement is false. Intel's counsel makes no reference as to where or when ACI made this statement, so ACI cannot counter with a proper citation.

At the oral hearing at the Court of Appeals, Intel's counsel broadened Intel's claim to include the Intel system, which those skilled in the art would say is absurd – not only for examples like the PCI clock above, but also if it were so, Intel would never have sold more than a few hundred systems rather than over a billion microprocessor products.

In its analysis on this point, the District Court finds that, despite testimony from ACI's expert (A0958: U) that the clock signal's delay due to passing through intermediate circuits is minimal and knowable (and within the tolerances specified by Intel), the delays of unknown duration prevent a predetermined relationship between these signals' origination and destination.

No expert testimony other than ACI's expert was supplied. Moreover, no fact witness is

competent to testify as to these matters as it has to do with the operation of Intel's circuit – not the invention. Therefore, the inventor's comments regarding this circuit operation are not competent testimony. Thus, if the District Court had viewed the facts in the light most favorable to ACI, it would have determined that ACI's testimony was not contested by any other competent witness, and therefore could not be discounted – at least at the summary judgment stage.

Apparently, the District Court substituted its own judgment for that of the expert witness. This constitutes a finding of a disputed fact, which is not proper in a summary judgment context. Again, the Court should deny the summary judgment on this basis or remand the case for a hearing on the factual issues.

CONCLUSION

For the reasons stated, the petition for a writ of certiorari should be granted.

Respectfully Submitted,

/s/

Michael P. Fortkort
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13164 Lazy Glen Lane
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Counsel for Petitioner, All Computers, Inc.

Dated: November 25, 2007

UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT

2007-1016

ALL COMPUTERS, INC.,

Plaintiff-Appellant,

INTEL CORPORATION,

Defendant- Appellee.

ORDER

NOTE: This *order* is nonprecedential.

UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT

ORDER

Before Newman, Circuit Judge, Rader, Circuit Judge, and Gajarsa, Circuit Judge.

A petition for rehearing having been filed by the Appellant,

UPON CONSIDERATION THEREOF, it is ORDERED that the petition for rehearing be, and the same hereby is, DENIED.

The mandate has already issued.

FOR THE COURT,

/s/_____
Jan Horbaly Clerk

Dated: 07/12/2007

cc: Michael P. Fortkort
Ruffin B. Cordell
ALL COMPUTERS V. INTEL CORP, 2007-1016
(DCT -1:04-CV-586)

NOTE: This disposition is nonprecendtial

United States Court of Appeals for the Federal Circuit

2007-1016

ALL COMPUTERS, INC.,
Plaintiff-Appellant

v.

INTEL CORPORATION,
Defendant-Appellee

JUDGMENT

ON APPEAL from the United States District Court for the Eastern District of Virginia.

In CASE NO(S). 1:04-CV-586

This CAUSE having been heard and considered, it is ORDERED and ADJUDGED: AFFIRMED See Fed.Cir. R. 36

Per Curiam (NEWMAN, RADER, and GAJARSA, Circuit Judges).

ENTERED BY ORDER OF THE COURT

DATED: MAY 18, 2007 /s/_____
Jan Horbaly, Clerk

IN THE UNITED STATES DISTRICT COURT
EASTERN DISTRICT OF VIRGINIA

ALEXANDRIA DIVISION

ALL COMPUTERS, INC., Plaintiff	)	
v.	)	CIVIL ACTION NO. 1:04-586
Intel Corporation Defendant	)	

FINAL JUDGMENT

This MATTER is before the Court on the joint stipulation of Plaintiff All Computers, Inc. and Defendant Intel Corporation dismissing the remaining counterclaims and requesting that summary judgment be final judgment. On June 7, 2006, the Court signed a joint stipulation that the parties drafted and submitted, dismissing all remaining counterclaims and making summary judgment a final judgment- From the foregoing, it is hereby ORDERED that JUDGMENT is ENTERED in favor of Defendant Intel Corporation and against All Computers, Inc.

The Clerk is DIRECTED to ENTER JUDGMENT pursuant to Federal Rule of Civil Procedure 58.

The Clerk is directed to forward a copy of this Order to Counsel.

Entered this 11th day of September, 2006.

Signed

/s/

Gerald Bruce Lee
United States District Judge

Alexandria, Virginia

B3

IN THE UNITED STATES DISTRICT COURT
EASTERN DISTRICT OF VIRGINIA

ALEXANDRIA DIVISION

ALL COMPUTERS, INC.,	)	
Plaintiff	)	
	)	
v.	)	**CIVIL ACTION**
	)	**NO. 1:04-586**
Intel Corporation	)	
Defendant)		

JUDGMENT

This MATTER is before the Court on Defendant Intel Corporation's Motion for Summary Judgment. In its previous Memorandum Opinion of February 9th, the Court granted Defendant's Motion for Summary Judgment. From the foregoing, it is hereby

ORDERED that JUDGMENT is ENTERED in favor of Defendant Intel Corporation and against All Computers, Inc.

The Clerk is DIRECTED to ENTER Judgment pursuant to Federal Rule of Civil Procedure 58.

The Clerk is directed to forward a copy of this Order to counsel.

Entered this 9th day of February, 2005.

Signed

/s/_____

Gerald Bruce Lee
United States District Judge

Alexandria, Virginia

CERTIFICATE OF COMPLIANCE WITH RULE 33.1

This petition complies with the word limitations of Rule 33.1(g)(i) of the Rules of the Supreme Court of the United States as it contains less than 9000 words, i.e., the petition contains exactly 4107 words, including footnotes, which has been calculated using the word count feature of Microsoft Office Word 2003 word processing program.

December 12, 2007

/s/ _____

Michael P. Fortkort

Counsel for Petitioner, All Computers, Inc.

CERTIFICATE OF SERVICE

I hereby certify that on December 12, 2007 I caused three copies of the foregoing PETITION FOR WRIT OF CERTIORARI to be served by first class mail delivery to each of the following:

Ruffin B. Cordell, Esq.
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202-783-5070

/s/
Michael P. Fortkort
Counsel for Petitioner, All Computers, Inc.

No. _____

In the

SUPREME COURT OF THE UNITED STATES

ALL COMPUTERS, INC.,

Petitioner,

v.

INTEL CORPORATION,

Respondent.

On Petition for a Writ of Certiorari to the United States Court Of Appeals for the Federal Circuit No. 07-1016

APPENDIX

C 1

IN THE UNITED STATES DISTRICT COURT
FOR THE
EASTERN DISTRICT OF VIRGINIA
ALEXANDRIA DIVISION

ALL COMPUTERS, INC., Plaintiff,)		
v.	)	CIVIL ACTION NO.
	)	1 :O4cv586
INTEL CORPORATION, Defendant.)	)	

MEMORANDUM OPINION

This matter is before the Court on Defendant Intel Corporation's (hereinafter, "Intel") Motion for Summary Judgment on all counts in the Complaint. Intel argues that it does not infringe any of the asserted claims of Plaintiff All Computers Inc. (hereinafter, "ACI") U.S. Patent No. 5,506,981 (hereinafter, "'981 patent") and further argues that ACI has not proven that anyone has used the combination of apparatus and method necessary to constitute infringement of its '981 patent.

ACI filed this case on May 20, 2004, alleging that Intel's sale of computer components including Pentium Processors infringe its '981 patent under theories of direct infringement, infringement by inducement, and contributory infringement. On June 9, 2004, Defendant answered Plaintiff's complaint, denying infringement under any theory, and asserting affirmative defenses and declaratory

judgment counterclaims for non-infringement, invalidity, and unenforceability.

The issues presented in this summary judgment motion are straightforward. ACI has sued Intel claiming that Intel's Celeron processor, when used in combination with other components, including a socket and a clock chip, infringes its '981 patent. ACI's '981 patent teaches replacing a processor on consumer laptop computers with an accelerator board containing a faster version processor installed in order to achieve better performance. As Intel does not perform the actual conversions, but instead sells potential replacement processors, ACI has accused Intel of infringement by inducement and contributory infringement. ACI claims that Intel has promoted on its website the replacement of the original Processor found in consumer laptop computers with its enhanced versions. ACI claims further that by promoting this replacement package Intel has knowingly induced or contributed to the infringement by others who perform the replacement. Intel argues in its Motion for Summary Judgment that the '981 patent teaches a replacement technique, i.e. using an accelerator board to mount the replacement apparatus, that is outdated and no longer used, as any replacement processors during the infringing period were plugged directly into the socket without using an accelerator board. Intel argues as a predictable consequence that ACI has failed to prove that anyone has replaced a processor in a laptop computer using the teachings of the patent.

The Court has performed a claim construction analysis and defined essential claims

terms in dispute, after full briefing by the parties. The Court therefore finds two issues before it for resolution;

1) First, whether the Intel Celeron processor when used in conjunction with a Universal Socket 370 and either the ICS 9248-87 or 9250-10 clock chip mounted on an accelerator board literally infringes any of Claims 1, 3 , and 5 of the ' 981 patent[2]

2) Second, whether ACI has presented evidence that the Intel Celeron processor has been mounted on an accelerator board and used in combination with a Universal Socket 370 and either the ICS 9248-87 or 9250-10 clock chip by a consumer in a laptop computer .

The Court, after considering the evidence presented by the parties in light of its claim construction finds for Defendant Intel on both issues.

The Court finds that Intel's Celeron processor used with other components mentioned above does not literally infringe directly, or by inducement or contributory, Claims 1 , 3 , and 5 of the '981 patent for these separate reasons;

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[2] By Court Order of October 21, 2004, Plaintiff was limited to proving infringement with the Celeron processor used in combination with the Universal Socket 370 and ICS 9250-10 or ICS 9248-87 clock chips. Further, Plaintiff was limited to asserting only Claims 1, 3, and 5 as they are the only claims identified in ACI's Rule 26 Federal Rules of Civil Procedure Initial Disclosures and thereafter.

1) none of the accused components are mounted on an accelerator board as required by each of the asserted claims,

2) the accused components and system do not have a first clock signal within the meaning of each of the asserted claims; and

3) the accused components and system do not have a first clock signal with a known phase relationship to the second clock signal within the meaning of each of the asserted claims.

The Court finds further that ACI has failed to present any competent evidence that anyone has combined the accused components and arguably infringed the '981 patent by doing so.

The absence of *evidence of an infringing apparatus having been built* pursuant to the teaching of the '981 patent is fatal to ACI's claim or infringement under any theory of infringement.

I. BACKGROUND

Plaintiff ACI is the owner by assignment of U.S. Patent No. 5,506,981 entitled "Apparatus and Method for Enhancing the Performance of Personal Computers." The '981 Patent is generally directed to an accelerator board that is used to replace a slower speed computer microprocessor with a higher speed one. The accelerator board, a printed circuit board on which the faster microprocessor and other components including a sub-harmonic generator and phase lock loop is mounted, connects via a socket to the computer system board. The

accelerator board generates a clock signal that is faster than, but still synchronized with, the original computer system clock signal. It does this by having the accelerator board mounted sub-harmonic generator communicate with the first clock signal that controlled the original but now replaced microprocessor, to create a synchronized sub-harmonic signal. The accelerator board mounted phase lock loop multiplies the sub-harmonic signal to generate a new faster clock signal for the upgraded microprocessor.

ACI is a Canadian company that designs and sells computer parts and circuitry. Defendant Intel corporation is a Delaware corporation that manufactures and supplies microprocessors, various chips, boards, systems, and software to the computer and communications industries.

The '981 Patent contains eight claims but ACI has asserted only claims 1, 3, and 5, set forth below.

Claim 1

In combination, a computer System board having a socket for a first microprocessor and a clock for generating a first clock signal intended for the operation of said first microprocessor;

an accelerator board connected to said socket to replace said first microprocessor;

said accelerator board having an upgrade microprocessor thereon for operation under the

control of a second clock signal having a frequency greater than that of said first clock signal;

means responsive to said first clock signal for generating sub-harmonic signal at a frequency that is a common denominator of the frequency of said first clock signal and said second clock signal with a known phase relationship between said sub-harmonic signal and said first clock signal; and

phase lock loop oscillator means responsive to said sub-harmonic signal for generating said second clock signal in known phase relationship to said first clock signal.

Claim 3

The combination of claim 1, wherein said accelerator board includes at least one of cache memory and local memory.

Claim 5

An accelerator board for use in replacing the microprocessor of a computer system board, said computer system board including means for generating a first clock signal at a first frequency for controlling the flow of digital information on said computer system board; said accelerator board comprising:

an enhanced microprocessor for operation by a second clock signal having a second clock frequency higher than said first frequency;

bus means for transmitting said first clock signal to said accelerator board;

a sub-harmonic generator responsive to said first clock signal for generating a sub-harmonic signal in known phase relationship with said first clock signal, the frequency of said sub-harmonic signal being a common denominator of said first clock frequency and said second clock frequency; and

a phase locked loop oscillator responsive to said sub-harmonic signal for generating a second clock signal at said second clock frequency in known phase relationship with said first clock signal for the operation of said upgrade microprocessor.

Before the Court are matters of both claim construction and summary judgment of non-infringement. The Court first addresses the construction of the claims, as a proper claim construction stands as a prerequisite to an infringement analysis.

II DISCUSSION

A. Claim Construction

Legal Framework

Claim construction is a question of law to be determined by the Court. *Markman v. Westview Instruments, Inc.*, 517 U.S. 370, 391 (1996). Under the Federal Circuit's framework, to ascertain the

meaning of a patent's claims, the Court must turn first to the intrinsic evidence within the patent, including the claims themselves, the written description, and the prosecution history. *CCS Fitness, Inc. V, Brunswick Corp.*, 288 P.3d 1359, 1366 (Fed. Cir. 2002) ("Claim interpretation begins with the claims themselves, the written description, and, if in evidence, the prosecution history."); *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996). When evaluating the intrinsic evidence, "[c]laim language generally carries the ordinary meaning of the words in their normal usage in the field of invention." *Invitrogen Corp. V. Biocrest Mfg.*, L.P., 327 F.3d 1364, 1367 (Fed. Cir. 2003). In fact, the court applies a heavy presumption that a claim term carries its ordinary and customary meaning as it would be understood by one of ordinary skill in the relevant art at the time of the invention. *Zelinski v. Brunswick* Corp., 185 F.3d 1311, 1315 (Fed. Cir. 1959).

Although reference to the language of the claims and the written description is paramount, *Digital Biometics, Inc. v. Identix, Inc.*, 149 F.3d 1335, 1344 (Fed. Cir. 1998), the prosecution history also provides a particularly helpful reference, as it "contains the complete record of all the proceedings before the Patent and Trademark Office, including any express representations made by the applicant regarding the scope of the claims." *Vitronics*, 90 F.3d at 1582-83.

Only where the Court remains unable to ascertain meaning from such intrinsic evidence should the Court then turn to extrinsic evidence, such as expert testimony. *Bell Atlantic Network Servs., Inc. V. Covad Communications Group, Inc.*,

262 P.3d 1258, 1269 (Fed. Cir. 2001). In most situations, resort to extrinsic evidence is unnecessary and improper as "an analysis of the intrinsic evidence alone will resolve any ambiguity in a dispute claim term." *Vitronics,* 90 F.3d at 1582.

Dictionary Definition

Dictionary definitions are also useful resources in determining a claim terms' meaning. Contemporary dictionary definitions are considered a reliable and objective source for determining claim terms ordinary and customary meaning at the time the patent issues. But the court is mindful that dictionary definitions must be viewed cautiously and carefully.

> . . . consulting dictionary definitions is simply a first step in the claim construction analysis and is another reason why resort must always be made to the surrounding text of the claims in question, the other claims, the written description, and the prosecution history. Our precedent referencing the use of dictionaries should not be read to suggest that abstract dictionary definitions are alone determinative. In construing claim terms, the general meanings gleaned from reference sources, such as dictionaries, must always be compared against the use of the terms in context, and the intrinsic record must always be consulted to identify which

of the different possible dictionary meanings is most consistent with the use of the words by the inventor.

Brookhill-Wilk 1 L,L.C, v. Intuitive Surgical, Inc., 334 F.3d 1294, 1300, 67 USPQ2d 1132, 1137 (Fed. Cir. 2003). See Also *Toto Co, v. white Consolidated Industries, Inc.*, 199 F.3d 1295 (Fed. Cir. 1999).

Definitions contained in technical dictionaries devoted to a specific discipline may be given greater weight than a general dictionary. *Transclean Corp. v. Bridgewood Services, Inc.*, 290 F.3d 1364 (Fed. Cir. 2002).

Dictionary definitions are to be rejected if they conflict with the language of the claim terms or specifications. *Renishen PLC v. Marpass Soeieta Per Aziona*, 158 F.3d 1243, 1250 (Fed. Cir. 1996).

Several of the terms found in the claims of the '981 patent are expressly defined in the written description, and other terms, although not expressly defined, are illustrated through examples in the written description and figures. Such definitions and examples have been helpful; however, the Court is aware that it must exercise particular care when interpreting claims in light of the specification, as "there is sometimes a fine line between reading a claim in light of the specification, and reading a limitation into the claim from the specification." *Comark Communications, Inc., v. Harris Corp.*, 156 F.3d 1182, 1186 (Fed. cir. 1998). Although it is improper to read a limitation from the specification into the claims, *Comark Communications* at 1186, "[c]laims must be read in view of the specification, of which

they are a part," *Markman*, 52 P.3d at 979, *see also United States v. Adams*, 383 U.S. 39, 49 (1966) ("[C]laims are to be construed in light of the specifications and both are to be read with a view to ascertaining the invention.")

Analysis

Patent infringement analysis is a two step process. First, the Court must construe the meaning of the asserted claims, See *Markman v. Westview Instruments, Inc.*, 517 U.S. 370, 371-73 (1996), and second, the Court must compare the properly construed claims to the accused system or device. *Ekchain v. Home Depot, Inc.*, 104 F.3d 1299, 1302 (Fed. Cir. 1997). A finding of infringement for any particular claim requires that each and every limitation of that claim be found in the accused product. *Allen Eng'g Corp. V. Bartell Indus., Inc.*, 299 F.3d 1336, 1345-46, 1357 (Fed. Cir. 2002).

A party may be liable for a finding of contributory infringement or infringement by inducement if it sells its infringing devices to an entity that combines them so as to directly infringe a patent claim. *See Linear Tech. Corp. v. Impala Linear Corp.*, 379 P.3d 1311, 1326 (Fed. Cir. 2004). Direct infringement is, however, a prerequisite for contributory infringement or inducement. Id.

B. Claim Terms Not in Dispute

The parties agree on the definitions of the following claim terms, as does the Court after reviewing their

claim construction and summary judgment briefs, and therefore the Court will not recite the support for these definitions.

1. computer system board a printed circuit board made of insulating material with the components of a computer system mounted thereon
2. socket
   a hollow device designed to receive the pin connectors located on the underside of a microprocessor
3. a sub-harmonic signal
   a signal at a frequency chat is a common denominator of the frequency of the first clock signal and the second clock signal
4. ommon denominator
   a common multiple of the denominator of a number of fractions
5. known phase relationship
   two signals that have a synchronous (meaning zero phase differences) or other predetermined fixed phase relationship
6. cache memory
   memory located on the accelerator board that stores data frequently accessed by the upgraded microprocessor for fast access
7. local memory
   memory located on the accelerator board and associated with the upgraded microprocessor
8. connected
   joined or linked together

C. Claim Terms In Dispute

The following terms are in dispute and the Court finds the proper definitions to be as follows.

1. clock

an electronic circuit that generates accurately timed pulses used for synchronization in a digital computer

The support for this definition lies in the description of the operation of the clock in the claims and in the following specification language.

> Slow speed system board B will normally include a continuously operational crystal clock that generates the clock signal SCLK intended to clock the ghost microprocessor originally present on board B. Many systems use a higher speed crystal clock and divide by 2 to generate SCLK, while some use a divide by K, where K might be normally 2 but is increased to 3 to slow the system clock for data transfers on an I/O expansion bus forming a part of the slow speed system board. This causes SCLK to be synchronously switched between two rates. The Sub-Harmonic generator 3, produces S-HCLK 23 which is a synchronized to SCLK as a low sub-harmonic of SCLK. This permits many different SCLK frequencies to be synchronized as different harmonics of S-HCLK. As an example a slow speed system board may use a 48 Mhz crystal clock and normally divide the clock by 2 to produce a 24 Mhz SCLK signal, but synchronously change SCLK to 16 Mhz for certain I/O operations by changing the divider to 3.

('981 Patent, Col 4:58 - 5:8)

This definition is also consistent with the definition provided by the following technical dictionaries.

> McGraw-Hill Dictionary of Scientific and Technical Terms (5th ed. 1994) clock: A source of accurately timed pulses, used for synchronization in a digital computer
>
> IEEE Dictionary (5th ed. 1993) clock; A device that generates sporadic signals used for synchronization.

2. first clock signal
the clock signal that is generated by a clock on the computer system board for the operation of the microprocessor

This definition is derived from the plain language of the claims as well as the following specification language.

> Slow speed system board B will normally include a continuously operational crystal clock that generates the clock signal SCLK intended to clock the ghost microprocessor originally present on board B.

('981 Patent Col 4:58-61)

Whether the first microprocessor is present or removed (ghost) the first clock signal is intended for the operation of the first microprocessor according to the specification language.

> In accordance with one aspect of this invention, an accelerator board plug-in replacement to the microprocessor socket of a

system board includes a sub-harmonic signal generator responsive to the clock signal of the system board. The sub-harmonic signal is selected to have a frequency that is a common denominator of the frequency of the system board clock and a clock signal for the operation of an enhanced microprocessor contained on the accelerator board.

('981 Patent Col 2:31-39)

The control signals on MP Control bus 22 will be recognized as part of the control signals of an 80386SX microprocessor. Given that this latter microprocessor has a different Address and Control timing than that of the ghost microprocessor, System Address Bus 26 is connected to the microprocessor 11 through Address Latch 10 and the MP Address Bus 28, the operation of which will be further described. In addition the change in microprocessor clock, causes the Data Bus timing of the new microprocessor and the slow speed system board to be different.

('981 Patent Col 4:41-50)

Considering as a whole a slow speed system board B and accelerator board 1 combined therewith, at start up a reset signal RSTIN is generated by board B and received on SS bus 20. RSTIN is synchronized according to state transition diagram FIG. 2b to form PRST which serves to reset microprocessor 11 and FPHI2 to track the internal phase of the microprocessor.

('981 Patent Col 5:40-47)

3. accelerator board

a printed circuit board made of insulating material that has an upgraded microprocessor mounted thereon and is adapted to connect into the socket of a computer board system

This definition is derived from the patent following specification language and figure 1.

> This invention relates to accelerator board devices that may be used to replace a microprocessor of a personal computer system which operates at a relatively slow speed in comparison to that of the replacement microprocessor to enhance the performance of the system.

('981 Patent Col 1:10-15)

> In accordance with one aspect of this invention an accelerator board plug-in replacement to the microprocessor socket of a system board includes a sub-harmonic signal generator responsive to the clock signal of the system board.

('981 Patent Col 2:31-34)

> Accelerator board 1 is used in conjunction with a slow speed system board B which will normally include a socket S for a microprocessor for which board B was designed, which microprocessor will be responsive to those signals on SS Bus 20 indicated above. In this case it will be recognized that these signals form pan of the control signals for

a 80286 microprocessor. This "slow" microprocessor is removed from the slow system board B and may be consequently referred to hereinafter as a ghost microprocessor. Accelerator board 1 includes pin connectors (not shown) which are receivable in socket S to interconnect SS Bus 20 to socket S; such pin connectors will also connect System Address Bus 25 and System Data Bus 27 to socket S to provide for the transfer of data between, the slow system board and microprocessor 11. The control signals on MP Control bus 22 will be recognized as part of the control signals of an 80386SX microprocessor. Given that this latter microprocessor has a different Address and Control timing than that of the ghost microprocessor, System Address BUS 26 is connected to the microprocessor 11 through Address latch 10 and the MP Address Bus 28, the operation of which will be further described. In addition the change in microprocessor clock, causes the Data Bus timing of the new microprocessor and the slow speed system board to be different.

('981 Patent Col 4:27-53)

For the purposes of this description it will be assumed that the ghost microprocessor for which the slow speed system board B was designed was an 80286 microprocessor operating at 16 Mhz, and that the microprocessor 11 of the accelerator board 1 is an 8038SX operating at a frequency of 48

> Mhz, to which microprocessors the timing diagram of FIG. 10 is applicable. For such system, the frequency of the sub-harmonic generator 3 is conveniently selected to be 4 Mhz, and the phase lock oscillator 4 accordingly to provide a value of N in the divide by N portion of the circuit of twelve.

('981 Patent Col 10:55-11:9 Fig 1)

The following dictionary definitions fully support the Court's definition of accelerator board.

> Dictionary of Computer and Internet Words (2001) accelerator board: A printed circuit board that can be added to a computer to enhance its performance by substituting a faster microprocessor without replacing the entire motherboard and associated components.

> Microsoft Computer Dictionary (4th ed. 1999) accelerator boards See accelerator card. A printed circuit board that replaces or augments the computer's main microprocessor, resulting in faster performance.

> Microsoft Computer dictionary (4th ed. 1999) daughterboard; A circuit board that attaches to another, such as the main system board (motherboard), to add extra capabilities.

> Microsoft Computer Dictionary (4th ed. 1999) board: An electronic module consisting of

chips and other electronic components mounted on a flat, rigid substrate on which conductive paths are laid between the components.

4. first microprocessor
the original microprocessor intended to be or mounted on the computer system board and receiving a first dock signal for its operation.

This definition is derived from the plain claim 1 language

> " . . . A computer system board having a socket for a first microprocessor
> and
> a clock for generating a first clock signal intended for the operation of said first microprocessor"

as well as the following specification language.

> . . . socket S for a microprocessor for which board B was designed, which microprocessor will be responsive to those signals on SS Bus 20 indicated above. In this case it will be recognized that these signals form pan of the control signals for a 80286 microprocessor. This "slow" microprocessor is removed from the slow system board B and may be consequently referred to hereinafter as a ghost microprocessor.

('961 Patent Col 4:29-35)

> Slow speed system board B will normally include a continuously operational crystal clock that generates the clock signal SCLK intended clock the ghost microprocessor originally present on board B.

('961 Patent Col 4:58-61)

5. upgrade microprocessor

> A microprocessor which operates at a faster speed than the first microprocessor

This term is defined in the following specification language.

> One way to increase the performance of a personal computer system is to replace the microprocessor in the system with a higher speed microprocessor operating on a higher clock rate, . . .

("981 Patent Col 1:19-22)

This definition is also fully supported by the following dictionary definition.

> Microsoft Computer Dictionary (4th ed. 1999)
> upgrade:
> n. The new or enhanced version of a products;
> v. To change to a newer, usually more powerful or sophisticated version.

6. sub-harmonic signal

> a signal at a frequency that is a common denominator of the frequency of the first clock signal and the second clock signal

This term is defined in the following specification language as well as figures l, 10, and 11 of the patent.

> The sub-harmonic signal is selected to have a frequency that is a common denominator of the frequency of the system board clock and a clock signal for the operation of an enhanced microprocessor contained on the accelerator board.

('981 Patent Col 2:35-39)

> The Sub-Harmonic generator 3, produces S-HCLK 23 which as synchronized to SCLK as a low sub-harmonic of SCLK. This permits many different SCLK frequencies to be synchronized as different harmonics of S-HCLK. As an example a slow speed system board may use a 48 Mhz crystal clock and normally divide the clock by 2 to produce a 24 Mhz SCLK signal, but synchronously change SCLK to 16 Mhz for certain I/O operations by changing the divider to 3. By using a Sub-Harmonic frequency of say 4 Mhz, both the 24 Mhz and the 16 Mhz SCLK frequencies can be synchronized, as well as other frequencies of which S-HCLK is a common denominator, such as 12, 20, 28 and 32 Mhz. The Sub-harmonic frequency S-HCLK is sent to Phase Locked Oscillator 4 which multiplies in a

standard Phase Locked Loop (PLL) fashion, the Sub-harmonic frequency by a whole number N to produce the high frequency clock signal PCLK for the new microprocessor.

('981 Patent Col 4:67-5:17)

7. sub-harmonic generator

the sub-harmonic generator in the circuitry identified in Figures 3 a and b of the '981 Patent and described in Col 6:28-63.

L2A; S-HCLK = /DELYI * /DELYO

L2B: DELYI = S-HCLK + DELYI * /DELYO

The Sub-Harmonic generator uses in addition to logic equations L2a and L2b, flip-flop 56 and delay line 58. Referring to the state transition diagram of FIG 3b, it should be noted that all eight possible states of the 3 variables S-HCLK, DELYI and DELYO are shown although two of the states can only occur as a result of the unknown state of flip-flop 56 at power-on. The explanation will begin at state (0,0,0); if this is not the state at power-on, the circuit will go through the state (0,0,0) within a few clock cycles of SCLK. From state (0,0,0), the circuit goes to state (1,0,0) on the next negative edge of SCLK and then immediately to state (1,1,0) . This means that S-HCLK goes from logic 0 to logic 1 follow by DELYI (input to the delay line) also going from logic 0 to logic 1. Since the time through the delay line is greater than the period of the

system clock SCLK, the next negative edge of SCLK changes the state to (0,1,0) with S-HCLK returning to logic 0. When the delay time from state (1,1,0) expires, DELYO (delay line output) goes to logic 1 moving the state to (0,1,1) and then immediately to state (0,0,1), DELYI going to logic 0. After a further delay time from state (0,0,1), DELYO goes to logic 0 bringing the state back to the starting point of (0,0,0) . At this point it should be noted that S-HCLK is pulsed to logic 1 for one period of SCLK per fixed time interval, as determined by two times the delay introduced in accordance with logic equation L2b and the delay line 58. In the example of a 4 Mhz S-HCLK signal, the time delay in accordance with logic equation L2b and delay line 58 is chosen or a minimum of 110 nanoseconds (ns) and a maximum of 120 ns. This produces a S-HCLK signal at a rate of 4 Mhz and synchronized to the slow system board clock SCLK for any of the following rates: 12, 16, 20, 24, 28 or 32 Mhz.

('981 Patent Col 6:28-63)

8. Phase lock loop oscillator means responsive to said sub-harmonic signal for generating said second cock signal in known relationship to said first clock signal. This phrase is a means-plus-function limitation with the function being to generate the second clock signal in known phase relationship to the first clock signal and the structure as identified in Figure 4 of the '981 Patent.

This definition is agreed to in principle by the parties, and support is found in the following specification language.

The Sub-harmonic frequency S-HCLK is sent to Phase Locked Oscillator 4 which multiplies in a standard Phase Locked Loop (PLL) fashion, the Sub-harmonic frequency, by a whole number N to produce the high frequency clock signal PCLK for the new microprocessor.

('981. Patent Col :12-18)

This definition is also fully supported by the following dictionary definition.

> McGraw-Hill Dictionary of scientific and Technical. Terms (5th ed. 1994) phase-locked loop: A circuit that consists essentially of a phase detector which compares the frequency of a voltage-controlled oscillator with that of an incoming carrier signal or reference frequency generator; the output of the phase detector, after: passing through a loop filter, is fed back to the voltage-controlled oscillator to keep it exactly in phase with the incoming or reference frequency.

III. FACTS FOUND NOT TO BE IN DISPUTE BY THE COURT

The following are relevant material facts as to which there is no genuine factual dispute that the Court considers in its Summary Judgment analysis.

1. Undisputed facts relevant to "Accelerator Board" element of claims

a. ACI names the ICS9250-10 clock chip as including the accelerator board limitation, ACI 10/9 Interrog. Resp. at 5, 8 (Ex. D, Intel's Summary Judgment Brief).

b. The accused system includes a computer system board made of a printed circuit board with components mounted thereon. ACI 10/9 Interrog. Resp. 4, 8 (Ex, D, Intel Summary Judgment Brief at 9); Plaintiff Computers' Reply Brief to Defendant Intel Corporations, Inc.'s (sic) Claim Construction Brief (Oct, 2004) at 1.

c. The accused system do not include a second printed circuit board. ACI 10/9 Interrog. Resp. at 1, 2, 5, 8 (Ex. D, Intel. Summary Judgment Brief); Deposition Transcript of William Mangione-Smith Oct. 2-3, 2004, (hereinafter "Smith Dep. Tr." at 90: 9-91:3 (Ex. G, Intel Summary Judgment Brief).

d. The 810E2 chipset is a collection of integrated circuit components mounted on the computer system board. Intel 810E2 Chipset Platform Design Guide Aug. 2002 (hereinafter, "810E2 spec."), at 18-21 (Ex. H, Intel Summary Judgment Brief).

e. The 810E2 chipset is designed to support the input/output operations of an associated microprocessor. 810E2 Spec. at 18-21 (Ex. H, Intel Summary Judgment Brief).

f. The 810E2 chipset does not include a clock chip of any kind. 810E2 Spec. at 139-141 (Ex. H, Intel Summary Judgment Brief).

2. Undisputed facts relevant to "First Clock Signal" element of claims

g. The ICS 9248-87 or ICS 9250-10 clock

chips are integrated circuit components manufactured by Integrated Circuit Systems, Inc. *See* ICS9250-10 Frequency Timing Generator for Pentium II systems at 1 (hereinafter, ICS9250-10 Spec) Ex. L, Intel Summary Judgment Brief)

h. The ICS 9248-87 or ICS 9250-10 clock chips are mounted on the computer system board of the accused system. ACI 10/9 Interrog. Resp. 5, 8 (Ex. D, Intel Summary Judgment Brief); *see* also ICS 9250-10 Spec. at 1 (Ex. J, Intel Summary Judgment Brief); ICS 9248-87 Spec. at 1 (E L, Intel Summary Judgment Brief).

i. ACI alleges that the "first clock igna1" of the claims in a signal internal to the ICS 9248-87 or ICS 9250-10 clock chips. ACI 10/9 Interrog. Resp. at 2 (Ex. D, Intel Summary Judgment Brief).

j. AC]: and its expert admit that the "first clock signal" terminates within the internal circuitry of the ICS 9248-87 or ICS 9250-10 clock chips. P1aintiff All Computers, Inc.'s Response to Intel Corporation's Second Set of Request For Admissions To Plaintiff (Nos. 360, 3G1) (Ex. I, Intel

Summary Judgment Brief) ; Smith Dep. Tr. At 150:12-19 (Ex. G, Intel Summary Judgment).

3. Undisputed facts relevant to 'Known Phase Relationship" element of claims

k. There are a number of buffers between the output of the block PLL1 on the ICS 9250-10 part and any PLL on the Intel Celeron microprocessor. Smith Dep. Tr. At 156:7-157; 16, 311:2l-313:10 (Ex. G, Intel Summary Judgment Brief).

l. Each buffer introduces a level of phase error. Smith Dep. Tr. Al: 156:7-157:16,311:21-313:10 (Ex. G, Intel Summary Judgment Brief).

m. ACI does not know what the phase relationship between the alleged first and second clock signals of the accused system. Smith p, Tr. At 160:20-l6l;4 (Ex. G Intel Summary Judgment Brief).

4. Facts Relevant to No Proof of Direct Infringement

n. There is no evidence showing any party has practiced the asserted claims. *See* ACI Disclosure (Ex. B, Intel Summary Judgment Brief); ACI 10/9 Interrog. Resp. (Ex. D, Intel Summary

Judgment Brief; Response to Fourth Set of Interrogatories from William Mangione-Smith, Oct. 19, 2004 at 3,4 (Ex. E, Intel Summary Judgment Brief). Expert Report of William H. Mangione- Smith Pursuant to the Federal Rules of

Civil Procedure Rule 26(2) (B), [sic, Rule 26(a) (2) (B)] (Ex. K, Intel Summary Judgment Brief).

IV. DOCTRINE OF EQUIVALENTS

Remarkably, ACI raised the issue of infringement by the doctrine of equivalents for the first time after the close of discovery. (Ex. E, Intel Summary Judgment Brief). No prior reference to the Doctrine of Equivalents had been made by although ACI's theory of infringement was required to be asserted in ACI's Rule 26 initial disclosures due July 30, 2003 (Ex. B, Intel Summary Judgment Brief), and also in ACI's responses to interrogatories timely made, and in its expert's disclosures timely made.

It incontrovertible that infringement under the doctrine of equivalents must be timely asserted in order to provide a defendant with the opportunity to conduct proper and often extensive fact and expert discovery.

A party's case is limited to its contentions and disclosures. *See Genentech, Inc. v. Amgen, Inc.*, 289 F.3d 761, 773-74 (Fed. Circ. 2002) (district court did not abuse its discretion by enforcing local rule requiring plaintiff to disclose whether infringement under doctrine of equivalents was being asserted by precluding party from offering evidence of infringement under such theory); *Masco Corp. of Indiana v. Price Pfister* 1994 U.S. Dist. LEXIS 20597, *4-*6 (E.D. Va. Oct. 7, 1994) (defendant is entitled to know plaintiff's contentions, both factual

and legal), aff'd 64 F.3d 676 (Fed. Cir. Aug 11, 1995) (per curiam)

This is because infringement under the doctrine of equivalents has its own test and requirements, and is not a lesser-included offense to literal infringement. *See* Zelinski v. *Brunswick Corp.*, 185 F.3d 1311, 1316 (Pad. Circ. 1999). It requires specific allegations and specific proof above and beyond that required for literal infringement. Id.; see also *Genentech*, 289 F.3d at 773-74. It often requires the testimony of a technical expert to determine whether there are only "insubstantial" differences between the accused device and that described in the claims. *See Warner-Jenkinson Co., Inc. v. Hilton Davis Chem. Co.*, 520 U.S. 17, 40 (1997); *Eagle Comtronics v. Arrow Communication Labs., Inc.*, 305 F.3d 1303, 1315 (Fed. Cir, 2002).

The Court therefore limited the Plaintiff's case to one of literal infringement, and further limited the products asserted to infringe to those disclosed timely by the Plaintiff.[2] Those products included the Intel Celeron microprocessor used in combination with a Universal Socket 370 and either an ICS 9248-87 or ICS 9250-10 clock chip.

V. Standard of Review - Summary Judgment

Under Federal Rule of Civil Procedure 56 (c), the court must grant summary judgment if the moving party

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[2]Court Orders dated October 21, 2004 and November 12, 2004.

demonstrates that there is no genuine issue as to any material fact, and that the moving party is entitled to

judgment as a matter of law. *See* Fed. R. Civ, P. 56(c). In reviewing a motion for summary judgment, the Court views the facts in the light most favorable to the non-moving party. *See Anderson v. Liberty Lobby, Inc.*, 477 U.S. 242, 255 (1996). Once a motion for summary judgment is properly made and supported, the opposing party has the burden of showing that a genuine dispute exists. *See Matsushita Elec. Indus. Co. v. Zenith Radio Corp.*, 475 U.S. 574, 586-87 (1986). The mere existence of some alleged factual dispute between the parties will not defeat an otherwise properly supported motion for summary judgment; the requirement is that there be no genuine issue of material fact. Anderson, 477 U.S. at 248. "Rule 56(e) requires the non-moving party to go beyond the pleadings and by [his] own affidavits, or by the 'deposition, answers to interrogatories, and admissions on file,' designate 'specific facts showing that there is a genuine issue for trial.'" *Celotex Corp. v. Catrett*, 477 U.S. 317, 324 (1986).

Differences over how the claims should be interpreted are not sufficient to avoid summary judgment since claim interpretation is a matter of law. *Phonometrics, Inc. v. Northern Telecom Inc.*, 133 F.3d 1459, 1464 (Fed. Cir. 1998).

Literal Infringement

In a literal infringement case such as this, the literal language of the claims controls the claim construction and infringement determinations, and in making those determinations, every word and phrase is considered material. *Perkin-Elmer Corp. v. Westinghouse Alec. Corp.*, 822 F.2d 1528, 1532-33 (Fed. Cir. 1987); *Lantech, Inc. v. Keip Machine Co.*, 32 F.3d 542, 546-47 (Fed. Circ. 1994); *TechSearch, L.L.C., v. Intel, Corp.*, 286 F.3d at 1371-73. For literal infringement, each limitation of the claim must be met by the accused device exactly, any deviation from the claim precluding a finding of infringement." *Lantech, 32 F.3d at 547.*

Therefore, the Court will review the Motion for Summary Judgement based on literal infringement of the products timely accused.

Accelerator Board

Intel argues that the term "accelerator board" requires an actual "board", while ACT states that the accelerator board must only consist of the components that go on the board, mainly those found in Claim 5. ACI's arguments are legally and factually unsupportable.

It is axiomatic in claim construction that a term in a particular patent must be defined consistently throughout in that patent. *Phonometrics, Inc. v, Northern Telecom, Inc.*, 133 F.3d 1459, 1465 (Fed. Cir. 1998). However, here, while both parties agree that the phrase "computer

system board" in the patent requires that a physical board exist, they differ on whether the "accelerator board" must have a physical board. The parties apparently are and the case law clearly requires that the claim preamble be included in the claimed invention. *Pitney Bowes, Inc. v. Hewlitt Packard Co., Inc.*, 182 F.3d 1298, 1305-06 (Fed. Cix, 1999).

Yet ACI, without support, asks the Court to erase the word "board" from "accelerator board".

ACI points to the prosecution history for support, but the plain reading of the examiner's reason for allowance is entirely consistent with the board being a necessary element of the claim.

> "... the prior art, either alone or in combination, does not teach an accelerator board with an upgrade microprocessor, means for generating a sub-harmonic signal at a frequency that is a common denominator of the frequencies of first and second clock signals, and a phase lock loop oscillator for generating the second clock signal in response to the sub-harmonic signal."

(USPTO Reason for Allowance Ex. 2, ACI Opposition to Summary Judgment) (Emphasis added)

Dr. Smith even admitted and then attempted to retract his opinion that the accelerator board contained a "board°. (Tr. 77:12-18, 78:4-81:20, Ex. G, Intel Summary Judgment Brief)

As previously noted, the "board" in accelerator board is required by law to be include in claim 1, 3, and 5, in order to read the claim terms consistently, absent the inventor changing the definition of this term within his patent. ACI cannot legally delete or somehow combine

terms.[3]

As the parties do not dispute that the accused Intel Celeron microprocessor is not mounted on an accelerator board, as there is no second printed circuit board (Smith Dep. Tr. at 90:9-91:3 Ex. G, Intel Summary Judgment Brief), the Court finds that Intel is entitled to summary judgment of non-infringement on all counts on this claim term alone.

First Clock Signal

Claim 1 of the patent recites the element "first clock signal intended for the operation of a first microprocessor and claim 5 recites the element "first clock signal . . . for controlling the flow of digital information". Intel argues that its accused system has no first clock signal as defined in the claims asserted.

ACI has responded with multiple arguments to the contrary, each reaching an unsuccessful dead end. (See undisputed facts section pgs 19-20; Ex. G H, Intel Summary Judgment Brief). Belatedly, in a declaration by Dr. Smith dated November 6, 2004, ACI argues that the Intel chipsets do include an external clock signal. His argument has no support, as previously noted herein, and the word-smithing in his affidavit is unfortunate.

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[3]ACI suggests that because the computer system board contains a "board", this also meets the requirements of the accelerator "board" element. The claim of the patent and specifications unquestionably call for separate boards and ACI's argument to the contrary is rejected. *Phonometrics, Inc.*, 133 F.3d at 14654.

Confronted with this problem, ACI has also asserted that the Intel BCLK is the first clock signal and the sub-harmonic signal. However, it cannot be both as the claims recite that the first clock signal generates the sub-harmonic signal, and as such they clearly are separate elements. *Phonometrics* at 1466-68.

Dr. Smith also stated in his first deposition that the first clock signal that controls the first microprocessor is the clock on the motherboard. However, ACI and Dr. Smith reluctantly agreed thereafter that Intel's chipsets signals do not emerge from their internal circuitry, so they cannot operate the first microprocessor or control the flow of digital information. (Tr. 150:12-19 Ex. G, Intel Summary Judgment Brief), (Spec. n. 1, Ex. L, Intel Summery Judgment Brief), (RFA Response 360-361 Ex. I, Intel Summary Judgment Brief).

The plain reading of the patent claims 1 and 5 (Claim 3 is dependent on Claim 1) demonstrate that there must be a first clock signal that has a known phase relationship with the sub- harmonic signal and the second clock signal. ('981 Patent Col 13:23-28, Col 14:12-22).

Clearly, from the plain claim language the first clock signal and sub-harmonic signal are separate signals, with the first used to generate the second.

All of ACI's attempts to locate an external first clock signal that operates the first microprocessor or is used for controlling the flow of digital information must therefore fail.

Finding no first clock signal as defined in the '981 Patent Claims 1, 3, and 5 in any of the accused systems, the Court finds non-infringement and GRANTS Summary Judgment as to all counts on behalf of Intel on this claim

term in dispute.

Known Phase Relationship

Each of the claims 1, 3, and 5 of the '981 Patent asserted in this lawsuit require the first clock signal to have a Known Phase Relationship with the sub-harmonic signal and the second clock signal ('981 Patent Col 13:20-28, Col 14:12-23). The parties agree and the Court has construed this phrase as meaning "two signals having a synchronous (meaning zero phase difference) or other predetermined fixed phase relationship".

The following undisputed facts are important in considering this claim element.

Richard M. Madter, inventor of the '981 patent, agreed with this definition when deposed. (Tr. at 84:2-9, 93:4-18, 108:16-109:4 Ex. O, Intel's Reply in Support of its Motion for Summary Judgment).

The specification calls for a synchronized phase relationship (`981 patent Col 2,43-53, Col 5:18-22). ACI has conceded that the first clock signal terminates within the clock chip in the Intel accused products (Dr. Smith Dep. Tr. at 150:12-19 Ex, G, Intel Summary Judgment Brief), (RFA Response 360-361 Ex. I, Intel Summary Judgment Brief). *See also* Ex. 1 Para. R, ACI's opposition to Intel's Motion for Summary Judgment).

Dr. Smith admitted in deposition that the first clock signal would have to travel through a series of circuits and wires which would delay the signal's arrival at the second clock chip an unknown duration (Tr. at 156:7-157:16, 311:21-313:15 Ex. G, Intel Summary Judgment Brief). Therefore, without a

predetermined delay time programmed into the system, which none of the accused systems contain, there cannot be a known phase relationship.

ACI's argument that the clock signal's delay will likely be minimal does not alter the uncontested facts recited above that there are delays of unknown duration that prevent a predetermined or synchronous relationship between these signals' origination and destination.

ACI's attempts in its opposition brief to qualify the clear language in the claims and specification is even contrary to the inventor's understanding of his patent, as explained above. As the Intel accused products do not have a "known phase relationship" within their system as required by claims 1, 3, and 5 of the '981 patent, the Court GRANTS Summary Judgment of non- infringement to Intel as to all counts on this claim term in dispute.

No Proof of Direct Infringement

Intel asserts that ACI has not come forward with any evidence of direct infringement of its accused products. ACI has responded through the affidavit of its expert Dr. Smith, stating that

> . . . On page 28 the memo suggests that there is some question as to whether any person ever upgraded an Intel processor to a faster version. This is ridiculous - the practice is so widespread and common that Intel encourages users to consider this option when making purchasing decisions. For example, the document http://www/intel.com/buy/tips.htm says `When buying a motherboard, consider a board that gives

> you the flexibility to upgrade or add a faster processor, more memory, another video card, and other core components.' Many other examples exist, contained in documents produced both inside and outside of Intel."

(Ex. 1, Para. W, ACI's Opposition to Intel's motion for Summary Judgment). This paragraph is revealing for several reasons. First, it is ACI's only "evidence" of direct infringement. Second, none of the "many other examples exist contained in documents both inside and outside of Intel·' were identified or produced in response to Intel's assertion'. Third, Dr. Smith perhaps carefully side steps the issue of whether Intel, in its website advertising, is urging buyers to consider future upgrades that include the purchase of microprocessors with built-in components versus the purchase of microprocessors mounted on acceleration boards.

Proof of direct infringement must be analyzed in accord with the claim construction arrived at and the products at issue. There is simply no evidence in this record that anyone has installed into a computer an infringing enhanced microprocessor mounted on an accelerated board. Dr. Smith's declaration is nothing more than supposition, containing no personal, or second hand, or circumstantial evidence that an infringing system was built. An expert's opinion without foundation is insufficient as a matter of law to constitute direct infringement. *Novartis Corp. v. Ben Venue*, 271 F.3d 1043, 1050-51 (Fed. Circ. 2002); *Arthur A. Collins*, 216 F.3d 1042, 1047-48 (Fed. Circ. 2000). The Court rejects Dr. Smith's unsubstantiated conclusory statement, as it must, and therefore finds no evidence of direct infringement by Intel's accused

products.

The finding of no direct infringement is dispositive of ACT'S claim of contributory infringement and infringement by inducement. Without direct infringement there can be no finding of infringement of either one. *Carborundum C. Innovations, Inc. v. Matter Metal Equipment*, 72 F.3d 872, 876 n. 4 (Fed. Cir. 1995); *Epcon Gas Systems, Inc. v. Bauer Compressors, Inc.*, 279 1022, 1033 (Fed. Cir. 2002).

The Court therefore GRANTS Summary

Judgment of non-infringement to Intel based on ACI's failure to come forward with competent evidence of direct infringement.

VI. CONCLUSION

For the foregoing reasons, it is hereby

ORDERED that Defendant Intel Corporation's Motion for Summary Judgment is GRANTED.

The Clerk is directed to enter judgment in favor of Intel Corporation and against All Computers, Inc. pursuant to Federal Rule of Civil Procedure 58, A separate Rule 58 Judgment Order will be entered with the Memorandum Opinion.

Entered this 9th day of February, 2005.

/s/_____
Gerald Bruce Lee
United State District Judge

Alexandria, Virginia